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APPLICATION NOTE

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Fitting the 5C180

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PROGRAMMABLE LOGIC APPLICATIONS
INTEL CORPORATION

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FITTING THE 5C180

CONTENTS

INTRODUCTION

In many ways, fitting the 5C180 is like climbing a mountain. Just when what appears to be the summit is reached, another summit is revealed behind it. This may occur several times before the actual summit is surmounted.

Likewise, fitting a 5C180 may have several false summits. Just when one has conquered what appears to be the "problem", another problem often appears behind it. This may occur several times before the design fitting is complete.

This application note addresses the problems that can be encountered when trying to fit a 5C180 and offers suggestions on how to get past them. The key to the climb is examining what resources are still available after the software* complains that a particular resource is not available.

SUMMIT NUMBER ONE: PIN ESTIMATE

Before keying in the design, it is best to estimate the I/O pin requirements. This is done by counting the total number of inputs to the device and outputs from the device.

PROBLEM: Not enough Input Pins

HELP: Run all synchronous clocks through Clock Buffers (CLKBs). Shared clocks may use the same CLKB output which may result in reduction from 4 CLK input pins to 1 CLK input pin (see Figures 1a &

*iPLS II ver. 1.1 or later is ESSENTIAL for 5C180 designs as the fitting algorithm was significantly improved with this release.
*iPLS II ver. 1.5 or later is HIGHLY RECOMMENDED as the error messages and Utilization Report Files were significantly enhanced with this release.

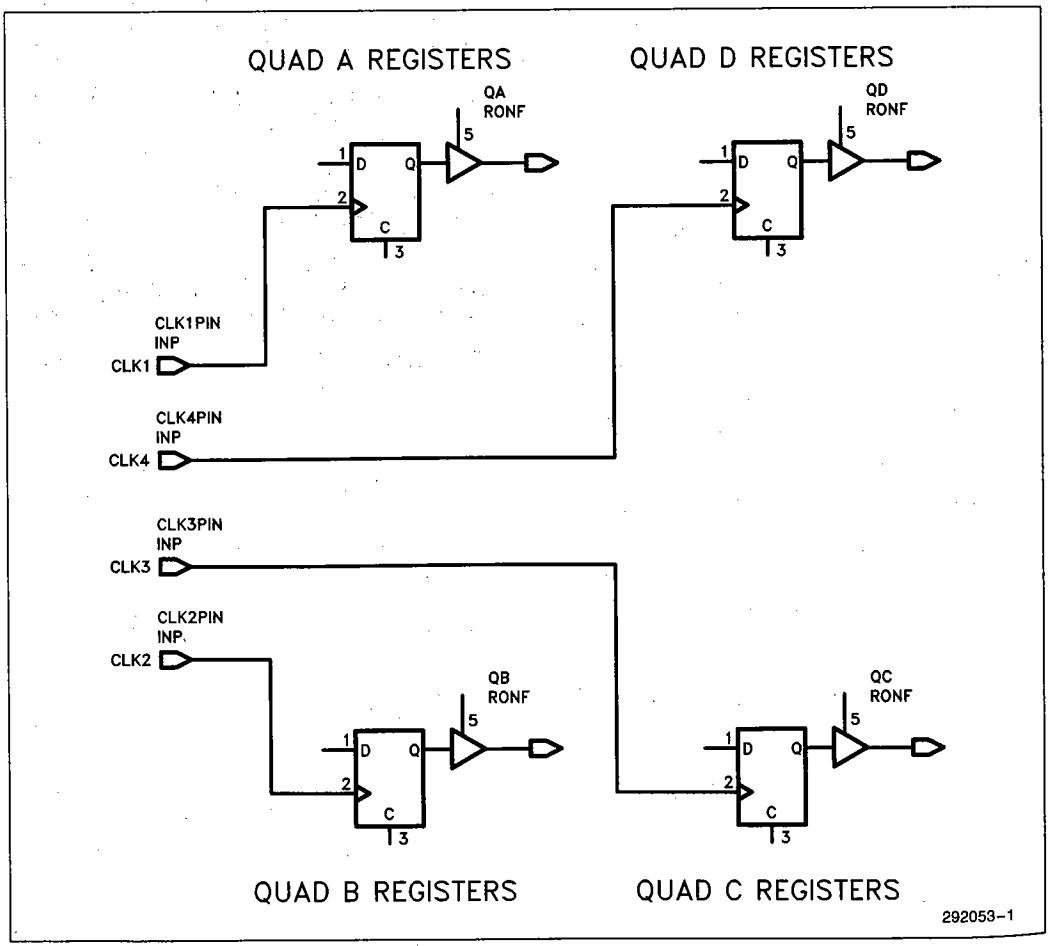


Figure 1a. Summit One—Input Clocks Before

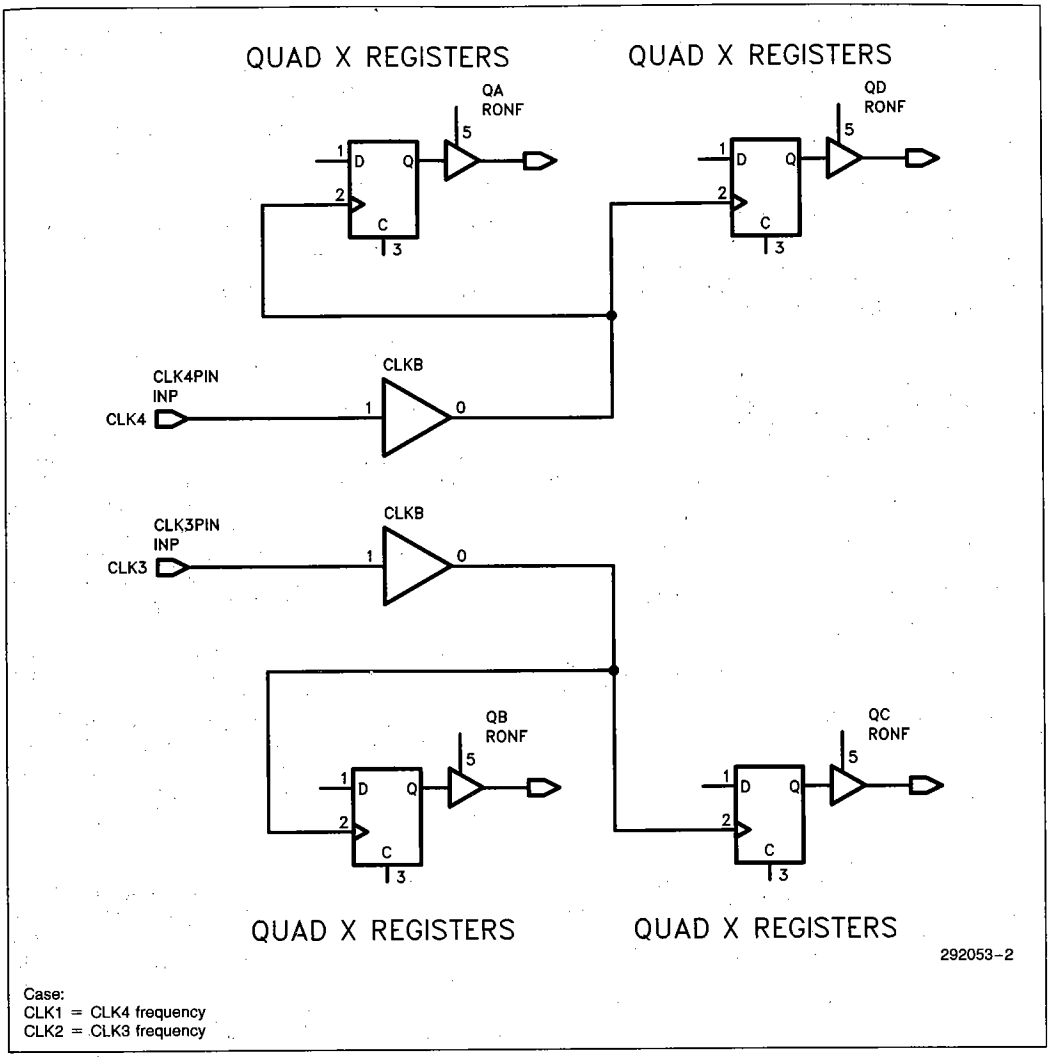


Figure 1b. Summit Two—Input Clocks After

1b). This also frees the registers that the clock feeds from the synchronous clock pin quadrant, increasing the chance of fitting later on. THIS PRACTICE IS RECOMMENDED FOR ALL DESIGNS.

PENALTY: Input setup time is shortened. (See Synchronous vs. Asynchronous A.C. Characteristics in Data Sheet).

If clock buffering cannot solve the problem, the design must be repartitioned to reduce the number of input pins. Repartitioning is explained in the next section.

SUMMIT NUMBER TWO: MACROCELL ESTIMATE

If the I/O pin requirements can be met, the next step is to consider the macrocell requirements. The total macrocell count can be estimated by counting the number of outputs plus the number of internal registers.

PROBLEM: Not enough macrocells

REPARTITIONING: Unless the fundamentals of the design can be changed, this error means that the design

must be repartitioned. This is done by removing part of the circuitry and placing it in a second device such as a 5C060 or 5C090. The 5C060 and 5C090 are recommended since their architectures (and therefore their ADFs) are nearly identical to those of the 5C180 (the NOCF and COCF primitives are the only exceptions).

Portions of the 5C180 ADF can be easily transferred into one of the smaller devices or the smaller device ADFs can be transferred back to the 5C180 if sufficient room is freed up later on. IT IS RECOMMENDED THAT FOUR OR FIVE UNUSED MACROCELLS BE LEFT IN THE 5C180 FOR USE BY LATER STAGES.

SUMMIT NUMBER THREE: SUCCESSFUL TRANSLATION

With the design entered, the next summit is successful translation.

ERROR: ***ERR-MAC-No macrofunction for: ...

EXPLANATION: The Macro Expander Module cannot find a macro for a network element.

FIX: Make sure correct search path is available for macro libraries. Check for typo or syntax error. If using schematic capture, make certain that only valid EPLD library symbols were entered.

ERROR: Any "***ERROR-XLT-..."

EXPLANATION: The Translator found a problem with the way the design was entered. These errors are basically syntax errors which violate ADF format. It may be a simple typo, missing parenthesis or missing semicolon. Remember that the iPLS II LOC does differentiate between upper and lower case letters. If using schematic capture, make sure that all device inputs and outputs have pin symbols and that all the pins and wires are properly labeled.

FIX: Refer to your iPLS II manual or call the EPLD Hotline, 1-800-323-EPLD, for help on the tough ones.

SUMMIT NUMBER FOUR: REGISTER CLOCK INPUTS

ERROR: ***ERROR-XLT-Clock input must be driven by INP or CLKB

EXPLANATION: The clock for a flip-flop must be driven synchronously by a direct quadrant clock pin input (INP) or asynchronously through a Clock Buffer (CLKB). This problem occurs when an equation or gate logic is connected directly to the register clock input.

FIX: In order to tell the LOC software that the clock for a flip-flop will be driven by an equation or gate logic, a Clock Buffer (CLKB) must be placed between the equation or logic and the register clock input for each register that is asynchronously clocked.

SUMMIT NUMBER FIVE: ASYNCHRONOUS CLOCKS AND OUTPUT ENABLES

ERROR: ***ERROR-XLT-OE with asynchronous clock not allowed

EXPLANATION: Asynchronous clock and output enable can't be used at the same time in the same macrocell. The 5C180 basic macrocell architecture, Figure 2, shows why. A single p-term is shared between the asynchronous clock and the output enable. This means that both switches in the diagram can be up or both switches can be down. By trying to use a p-term output enable with an asynchronous clock, the top switch would have to be down while the bottom switch is up. This cannot be done as then the register would be clocked and enabled with the same signal.

WORKAROUND: To get around this problem, one of the signals must be routed through another macrocell (see Figures 3a-b). The clock could be generated in another macrocell, sent out to a pin, then sent back in on the synchronous clock pin. Alternately, in a first macrocell the register is placed as an asynchronously clocked NORF. In a second macrocell, the register feedback is sent out to a pin using a CONF enabled by the desired enable signal.

PENALTIES: Routing the clock through a separate macrocell and back in offers slightly better performance—since the synchronous clock to ouput time is faster than a second macrocell delay, but this implementation uses a lot of resources—three pins and two macrocells. The second method, routing the feedback from the register back and controlling the output enable in a second macrocell is more straightforward and uses less resources.

SUMMIT NUMBER SIX: GREATER THAN ONE PRODUCT-TERM REGISTER CONTROLS

ERRORS: ***INFO-FIT- Eqn. too big, 4/-1 PTerm(s), on OE signal OE3

***INFO-FIT- Illegal inversion of CLEAR input (CLR1)

EXPLANATION: As shown in the basic 5C180 macrocell architecture, Figure 2, only one product term (multiple input AND gate) is available for the register

clock, clear, and output enable. This means that any control resource containing an OR gate following Boolean minimization will not fit. Likewise, any control resource requiring an invert will not fit either. To find the offending signal, LOOK AT THE EQUATIONS SECTION OF THE LOGIC EQUATION FILE (.LEF).

WORKAROUND: Onçe the offending signal has been located, it must be routed through another macrocell using an NOCF primitive (see Figure 4a-b). If the control signal is a clock, then a clock buffer (CLKB) must also be added.

PENALTY: Unless a trick explained below can be used, this routing results in the use of an additional macrocell and a doubling of the signal propagation delay.

Clr Fitting Trick

PROBLEM: Register clear input breaks 1 p-term resource limit

TRICK: If register has D input of either VCC or GND, substitute SR Flip-Flop.

EXPLANATION: D-type EPLD register has only 1 AND gate feeding CLR; SR Flip-Flop utilizes logic array for CLR input allowing a max of 8 AND gates (p-terms) for the CLR resource.

PENALTIES: SR Flip-Flop is synchronously clocked. D register has asynchronous clear.

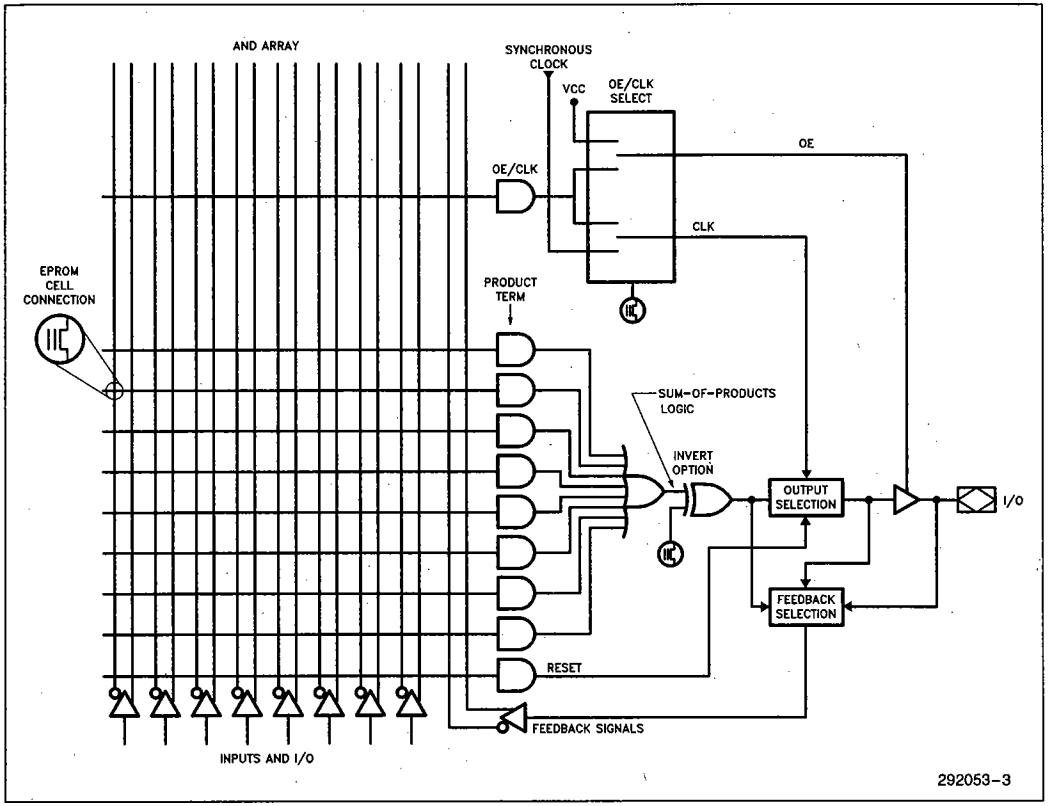


Figure 2. Basic Macrocell Architecture of the 5C180

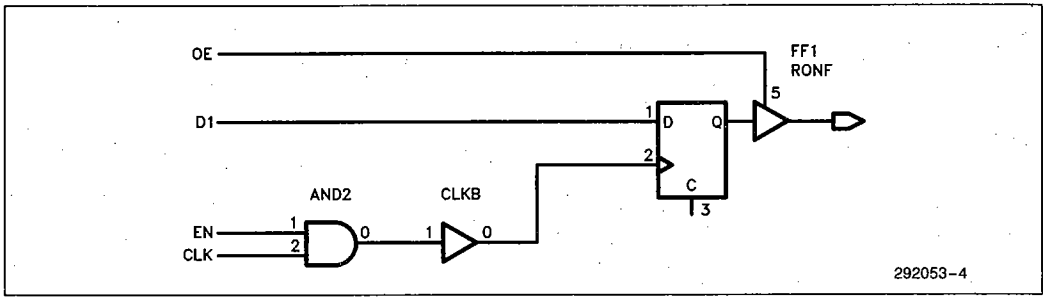


Figure 3a. Summit Five—Asynchronous Clock and OE Before

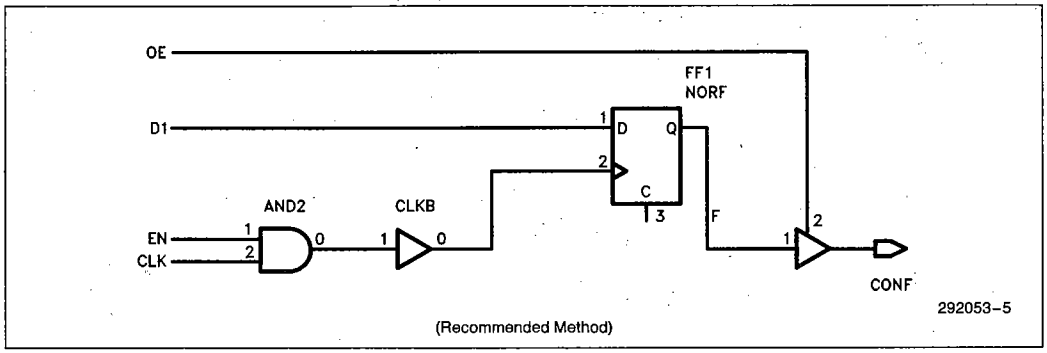


Figure 3b. Summit Five—Asynchronous Clock and OE After

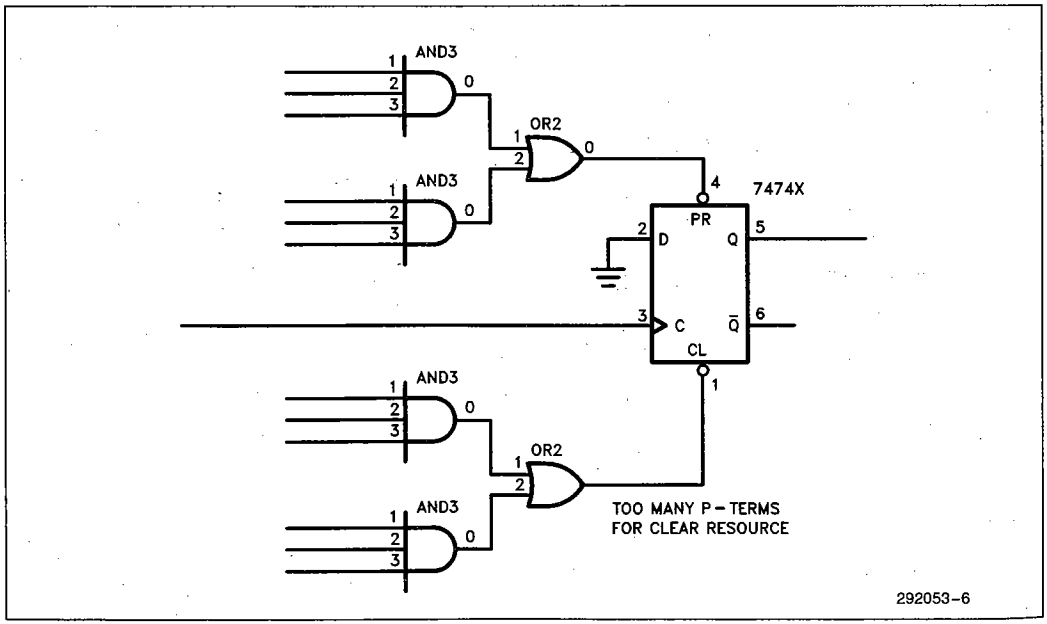


Figure 4a. Summit Six—Too Many P-Terms on Control - Clear

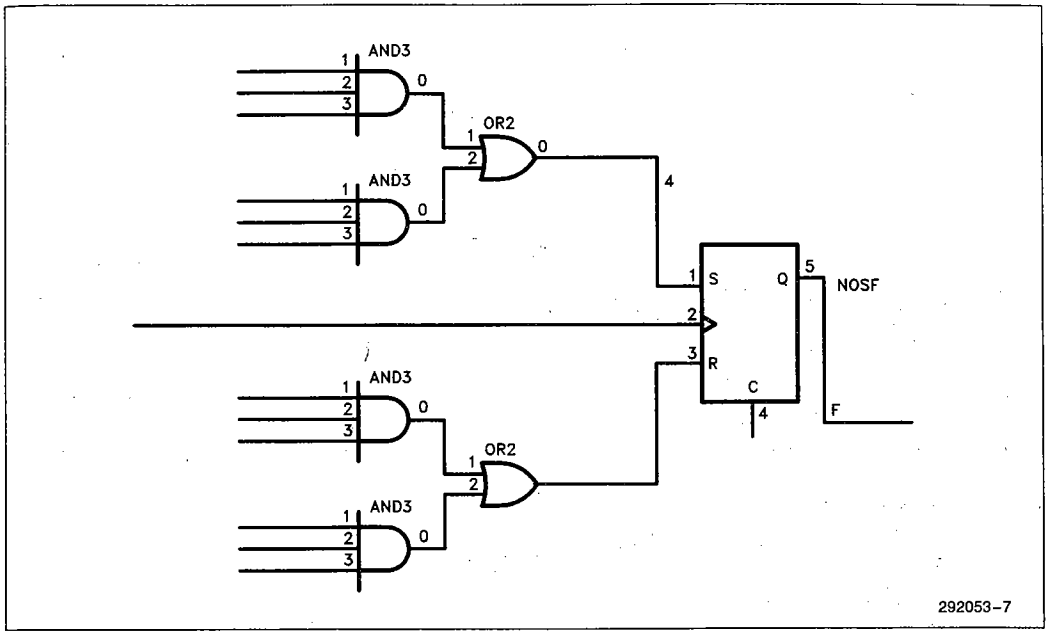


Figure 4b. Summit Six—SR Flip-Flop Equivalent Implementation

OE Fitting Trick

PROBLEM: Output enable on an equation or combinational equation exceeds 1 p-term resource limit.

TRICK: If a low output rather than a tri-state output can be tolerated, the signal can be gated rather than tri-stated.

EXPLANATION: Run the OE and the equation through an AND gate before going to a pin. The output of the pin will only follow the equation when the enable is active, otherwise it will be zero.

PENALTY: Forced low rather than tri-state output.

SUMMIT NUMBER SEVEN: NOT ENOUGH P-TERMS FOR AN EQUATION

ERROR: ***INFO-FIT- Too many PTerms to fit in any MCell: 10/8 for EQN.

EXPLANATION: Since the 5C180 has a maximum of eight product terms per macrocell, there's a chance that this number may be exceeded by the requirements of an equation. If so, the equation is cited by the LOC and can be examined by looking at the EQUATIONS section of the .LEF.

WORKAROUND: The workaround for this situation may already be in place! If any portion of the logic (or equation) is routed into an NOCF or CONF elsewhere in the design, that feedback can be taken and routed into the equation (see Figure 5a-b). This means a single feedback node—rather than several nodes will now feed the equation and thereby reduce the p-term count. (If the feedback is to be taken from a CONF primitive, the CONF must be changed to a COCF or COIF to make the feedback available.)

If part of the logic or equation is not routed into a NOCF or CONF elsewhere in the design, then part of the equation must be routed through a NOCF, COCF, or COIF primitive. A NOCF is recommended as it does not use a pin if placed in a global macrocell. If several equations are in violation of the eight p-term maximum, try to choose a group of logic that is common to all of the equations. In this manner, the p-term count for several equations can be brought down with the use of single extra macrocell, rather than the use of a macrocell for each equation.

PENALTY: Any time a portion of an output signal must be routed through another macrocell a speed penalty is incurred (roughly one propagation delay). If an already existing macrocell can be found, then there is no architectural penalty. If a new one must be created, then another macrocell is added to the total macrocell count.

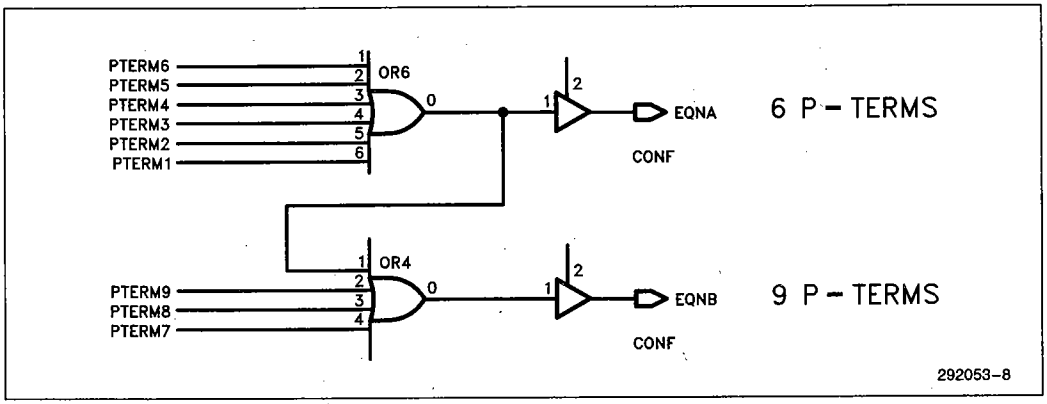


Figure 5a. Summit Seven—Too Many P-Term Equation Before

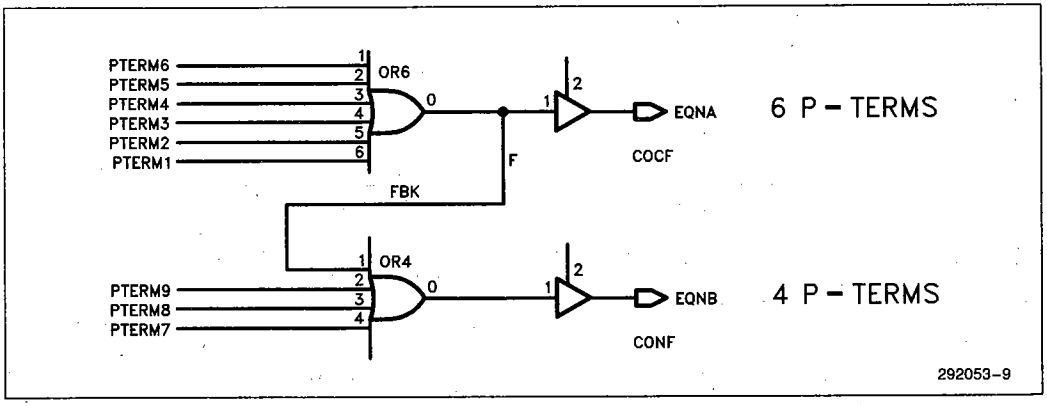


Figure 5b. Summit Seven—Too Many P-Term Equation After

SUMMIT EIGHT: MACROCELL RESOURCES EXCEEDED

ERROR: ***INFO-FIT- Design requires too many macrocells

EXPLANATION: If this error didn't occur at the beginning, there's a good chance summits five, six or seven will push the macrocell count over the limit. (Remember that the macrocell count includes not only the outputs, but also the buried resources such as NOCFs, NORFs and NOTFs). To find out exactly how many macrocells the design requires, LOOK AT THE NETWORK: SECTION OF THE LOGIC EQUATION FILE (.LEF). The inputs list in the LEF will list both the outputs and all the buried resources required by the design. If the count exceeds 48, then too many macrocells are required.

FIX: Repartition. The same applies if the number of input pins is exceeded.

THE FINAL ASCENT: NOT ENOUGH GLOBAL FEEDBACK!

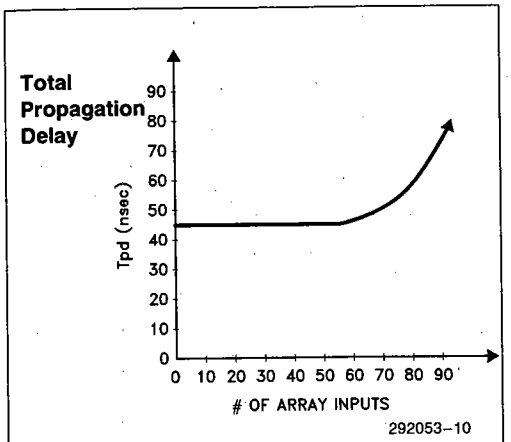
Congratulations! If you have made it this far, you have demonstrated courage, intelligence and tenacity beyond that of the average climber. You will soon be rewarded, but first there is one more obstacle to be overcome. Welcome to the North Face of local/global feedback!

A Word About Local/Global Feedback

First of all, why does local/global feedback exist? The answer can be found in the graph shown in Figure 6. The propagation delay versus array size is shown for the 5C060/090/180 family. As the number of inputs into the array increases, the propagation delay increases...exponentially. If all the inputs and feedback were made global, the 5C180 would have 136 inputs feeding each array (remember that both true and complement polarities must be fed into the array of a PLD architec-

ture). This would have put the 5C180 Tpd in the 250 - 300 ns range! By making eight macrocells local for four quadrants, the number of array inputs was dropped to 88 and the Tpd subsequently decreased to 75 ns.

The tradeoff to the local/global routing scheme is more difficult design routing. With the help of the iPLS II and a couple of tricks, however, most designs can still be fit.



Array Size

Device	Array Inputs	T_{PD}
5C060	40	45 ns
5C090	72	50 ns
5C180	88	75 ns

Array size increases Capacitance
Capacitance increases Propagation Delays

Figure 6. Propagation Delay vs. Array Size for the 5C060/090/180 Family

A Few Notes

The global/local macrocell assignments are shown in Figure 7. Please note that:

1. Dedicated input pins are GLOBAL.
2. Global macrocell I/O pin are GLOBAL.
3. Global macrocell internal feedback paths are LOCAL.
4. Local macrocell pin/feedback paths are LOCAL.

where GLOBAL means that the signal feeds all macrocells and LOCAL means that the signal only feeds the macrocells in its quadrant.

Clock Input Pins

The clock input pins feed the global bus like the regular inputs, except the synchronous register input connection is dedicated to a particular quadrant. Thus, each clock input can be used as a logic input in all quadrants or a clock input in its own quadrant. To be used as a register clock input in a quadrant outside its own, however, it must be tapped from the global bus via an asynchronous clock buffer (CLKB).

Global Macrocell Feedback

The feedback path is local for GLOBAL macrocells while the I/O input is global for all GLOBAL macrocells. Thus, changing the feedback of a register or combinational equation from a standard feedback to I/O pin feedback path will change the routing from local to global. The iPLS II LOC automatically recognizes and performs this through a process called "promoting". With the promotion process, global routing can be obtained on signals that would otherwise remain local.

***INFO-FIT- Promoted "TEQNf" from NOCF to COIF

Burying a Register in a Global Cell

Because the global macrocells have separate register and I/O pin feedback paths, it is possible to "bury" a register or equation by disabling the output buffer and still use the pin as an input. The iPLS II LOC automatically assigns an input to the pin of a buried register macrocell if it is necessary and possible. Such assignments are documented in the Utilization Report File (.RPT). If manual assignment is desired, it may be performed by placing the input pin assignment in the ADF INPUTS: list and assigning the buried register feedback to the same pin in the OUTPUTS: list (Figure 8). Registers or equations can only be buried on global macrocells, since local macrocells only have one feedback path that is used for either the register or the pin feedback.

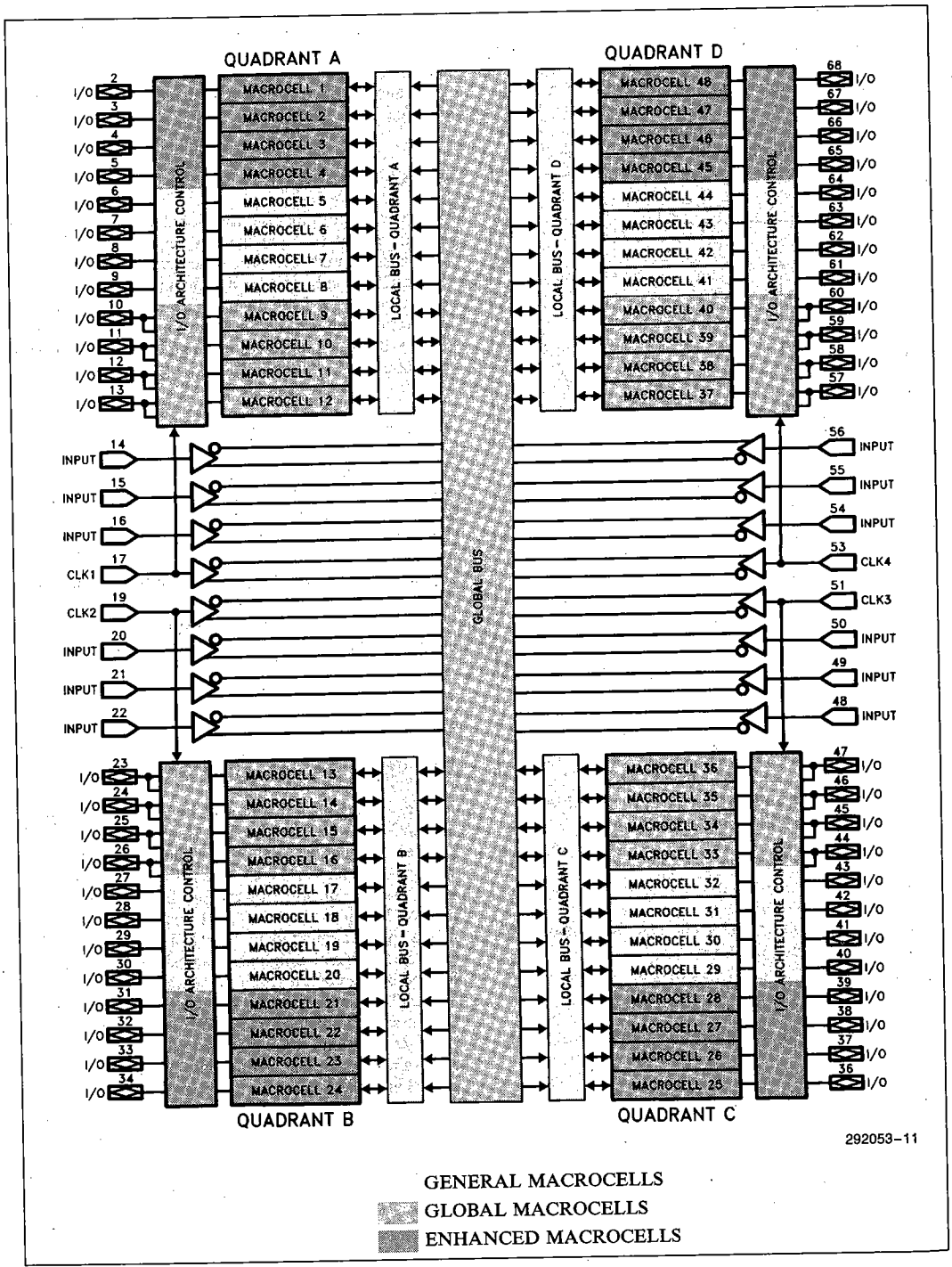
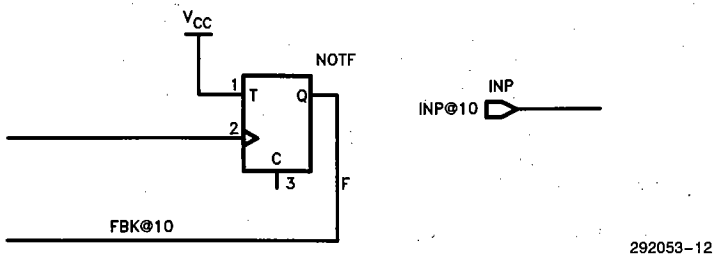


Figure 7. 5C180 Block Diagram



Buried Register Pin Assignment in ADF

```
Intel
PLDO Apps
July 27, 1988
5C180 Buried Reg Pin Assignments

PART: 5C180
INPUTS: A@15, B@10, CLK@17  % Assign input B to pin 10 %
OUTPUTS: FBK@10             % Assign buried reg feedback FBK %
                            % to pin 10 (GLOBAL macrocell 9) %
NETWORK:

A = INP(A)                  % Inputs %
B = INP(B)
CLK = INP(CLK)

FBK = NORF(IN,CLK,GND,GND)  % Buried Register %

EQUATIONS:

IN = A * B * FBK;           % Register Input Equation %

END$
```

Figure 8. Assigning Buried Reg in Schematic

Two Global Fitting Tricks

If the LOC is unable to fit the design, there are a couple of manual tricks that may help:

PROBLEM: NOT ENOUGH GLOBAL FEEDBACK

RESOURCES AVAILABLE: EXTRA MACROCELLS

TRICK: Duplicate the macrocell logic that needs to be global in two (or more) regions with appropriate renaming (see Figure 9).

EXPLANATION: This makes the signal available in two regions via two local macrocells rather than one which can't be global.

PENALTIES: There may be a slight timing discrepency between the two macrocells for combinational logic, but any discrepency will be small (< 2 ns).

PROBLEM: NOT ENOUGH GLOBAL FEEDBACK

RESOURCES AVAILABLE: EXTRA INPUT PINS

TRICK: Send out the signal that needs to be global and externally connect it to one of the input pins.

EXPLANATION: Inputs feed the global bus, making the signal available in all quadrants.

PENALTIES: An output buffer plus input buffer minus feedback delay is added (approximately 25 ns). An external connection must be made on the board.

NOTE:
For the previous tricks, look at the Utilization Report (.RPT) file. The "Interconnect Cross Reference" is particularly useful for examining the routing requirements of the design.

If the previous tricks cannot be done (see Figure 11) and scrutinization of the Interconnect Cross Reference reveals no other way to achieve the desired routing, repartitioning is necessary. That is, place a chunk of interconnected logic into a 5C060 or 5C090 and go back to the start.

CONCLUSION

Fitting the 5C180 is a process with many stages. One difficulty may hide the next and fixing one problem will sometimes uncover another. Equipped with the iPLS II LOC and a few tricks, however, fitting can be accomplished.

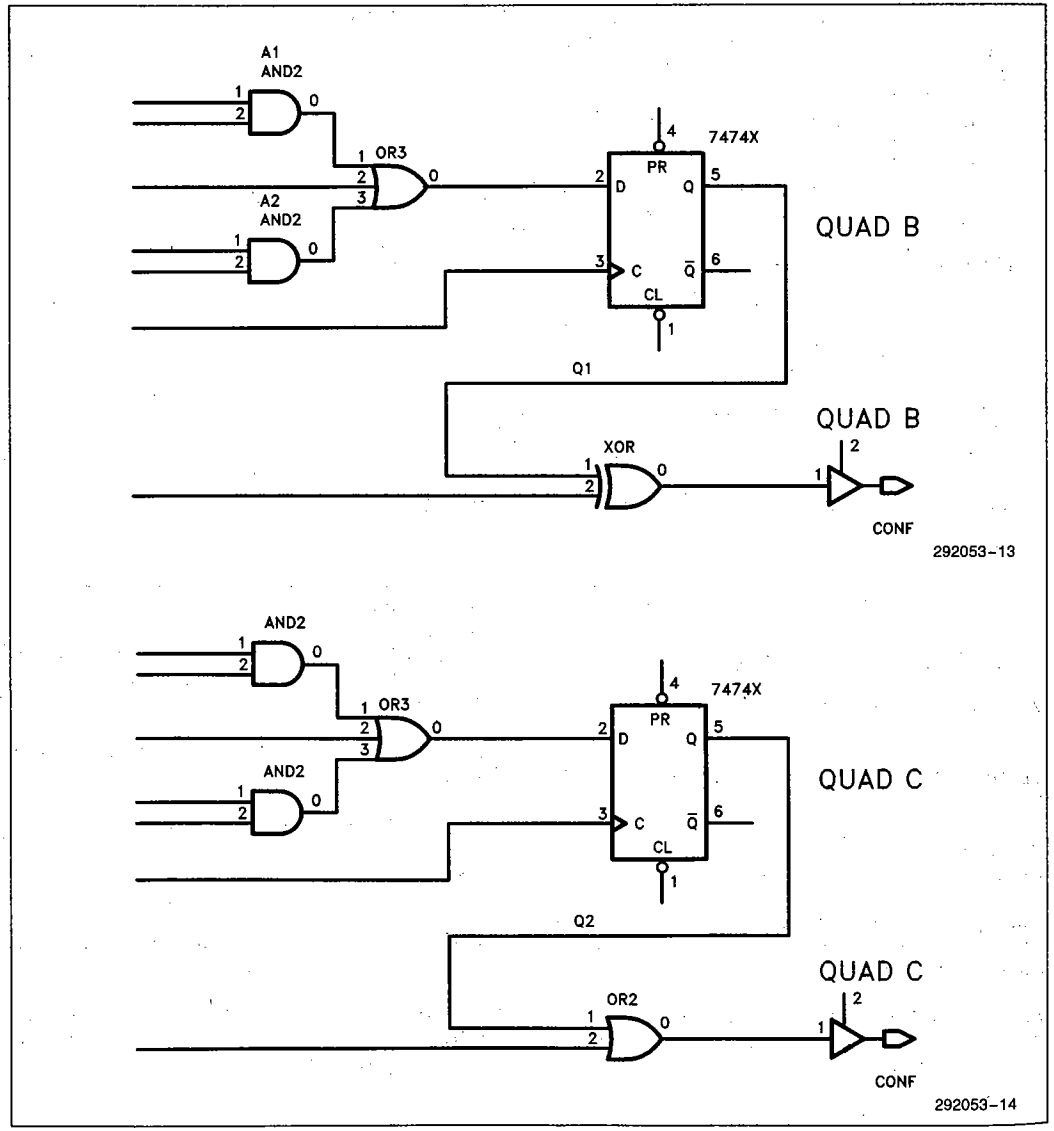


Figure 9. Not Enough Global Feedback Extra Macrocells—Fit

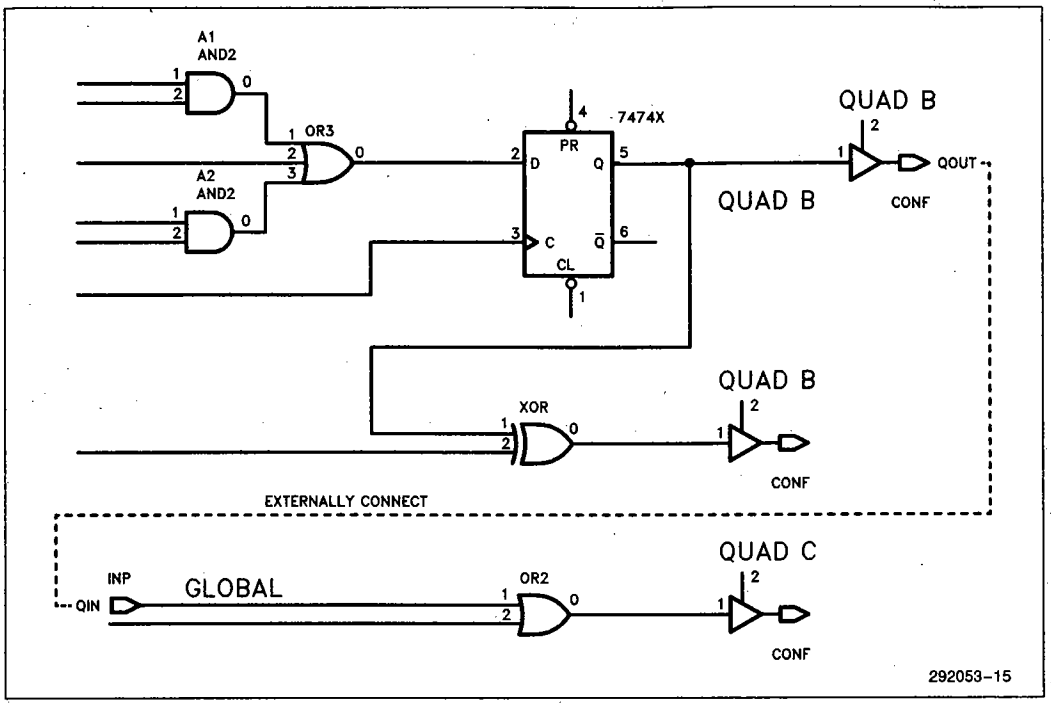


Figure 10. Not Enough Global Feedback Extra Inputs—Fit

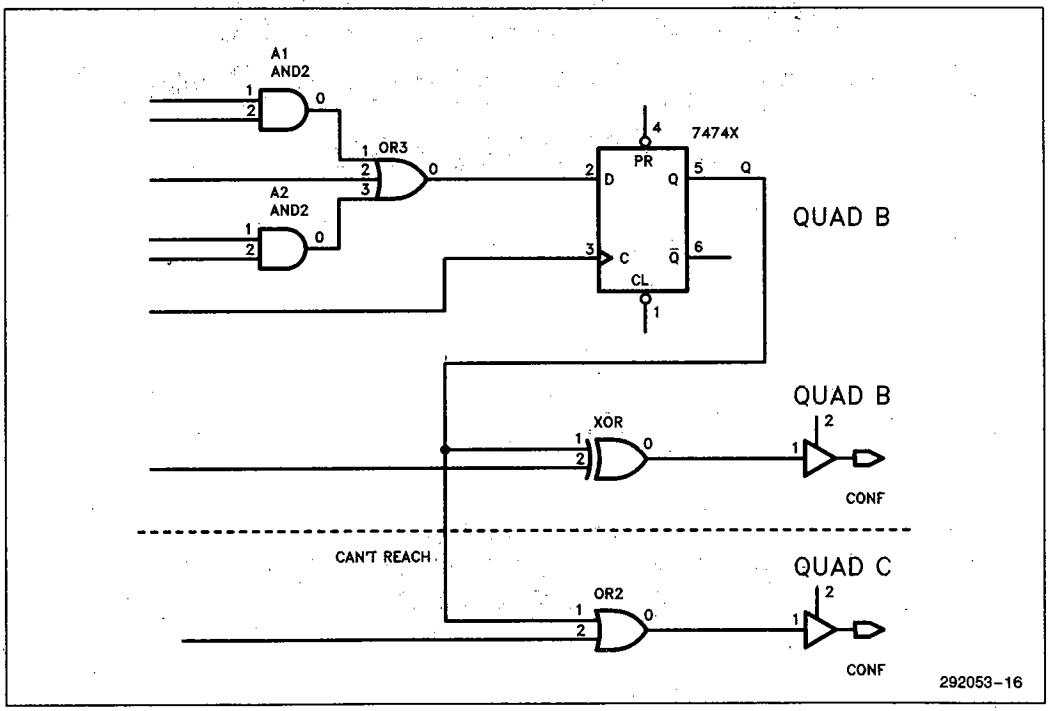


Figure 11. Not Enough Global Feedback—No Fit